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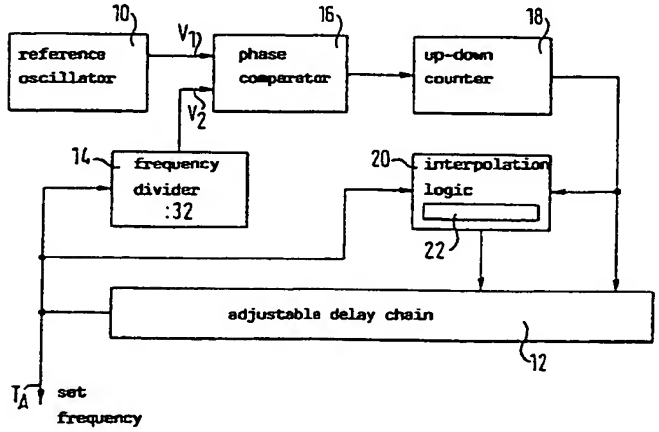
(54) A clock generator and phase comparator for use in such a clock generator.

(57) 1. A clock generator contains a reference oscillator (10), a digital closed delay chain (12), a digital frequency divider (14) and a digital phase comparator (16). The frequency divider (14) is connected between the output of the adjustable delay chain (12) and one input of the phase comparator (16). The output of the reference oscillator (10) is connected to a further input of the phase comparator (16). Between the output of the phase comparator (16) and the delay chain (12) a digital up-down counter (18) is connected, the counting direction of which is determined by the output signal of the phase comparator (16) and by means of which the corresponding length of the delay chain (12) is adjustable.

FIG. 1



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The invention relates to a clock generator of the kind as stated in the preamble of Claim 1; it also relating to a digital phase comparator according to the preamble of Claim 15 for use in such a clock generator.

With conventional clock generators of the aforementioned kind a voltage-controlled oscillator is provided as a rule as the adjustable oscillator, a low-pass filter being additionally connected between the voltage-controlled oscillator and the phase comparator. In turn the output of the voltage-controlled oscillator is fed back to an input of the phase comparator to achieve a phase-locked loop (PLL).

Of disadvantage in this respect is in particular the large number of external components needed. In addition, the analog functional units employed - such as phase detector, low-pass filter and the voltage-controlled oscillator - have a relatively complex configuration. In conclusion, the current consumption of such an analog clock generator is also relatively high.

The object of the invention is to create a clock generator together with a suitable phase comparator of the aforementioned kind which despite its simpler configuration and relatively low current consumption ensures reliable operation, permitting a more or less precise adjustment of the frequency in each case.

This object is achieved by the adjustable oscillator being a digital delay chain, the frequency divider being a digital programmable frequency divider and by connecting between the output of the phase comparator and the delay chain a digital up-down counter, the counting direction of which is determined by the output signal of the phase comparator and by means of which the corresponding length of the delay chain is adjustable.

On the basis of this configuration it is achieved that - apart from the oscillator quartz crystal for generating the reference frequency - external components are no longer needed. Apart from the bias generator required for current control in the sections of the chain no further functional units are provided. Accordingly, by extremely simple means a practically all-digital integrated structure of the clock generator is possible. A clock generator such as this is furthermore relatively insensitive to fluctuations in the supply voltage as well as to changes in temperature and fabrication tolerances. The output clock signal in each case can be adjusted with very high frequency accuracy. The frequency-sensing locked loop according to the invention is achieved by a system of the first order having extremely fast response.

The delay chain is preferably assigned an interpolation logic comprising a dual counter which is clocked by the output signal of the delay chain. The count of this dual counter is combined with the value of a number of least-significant bits of the output signal of the up-down counter to define, as a function of the value of these least-significant bits, the number of changes in the length of the delay chain by one step at a time for each clock cycle whilst the remaining most-significant bits directly address the delay chain.

By means of such an interpolation logic it can be assured in particular that changes in the length of the delay chain occur within the same time frame.

In one embodiment of the delay chain according to claim 3 the corresponding length of the delay chain and thus the frequency in each case can be adjusted by activating a corresponding loop inverter which defines the inversion point in each case at which the forward branch of the delay chain is directly connected with the return branch thereof.

Addressing the corresponding loop inverter is possible, for example, via the control inputs as stated in claim 4, it being good practice to undertake addressing so that only one loop inverter of the delay chain is activated at any one time.

Resetting the delay elements as defined by function, for instance on power up, is ensured in particular by the delay chain having preferably alternating delay elements of a first kind, the outputs of which are logical 0 in the reset condition, and delay elements of a second kind the outputs of which are logical 1 in the reset condition. Accordingly all connecting points of the delay chain can be reset, if required, to a precisely defined initial status, the output of the selected loop inverter assuming the correct value so that unwanted signal spikes are avoided when changes are later made to the length of the chain.

The maximum frequency step from one delay element to the next should possibly not exceed 1/6. Accordingly it is good practice to compose the delay chain of at least 6 delay elements.

On top of this the delay elements inserted with increasing chain length may have a higher delay than necessary for a shorter chain length and thus, in particular, the change in frequency as a percentage in the transfer from one delay element to the next may be maintained constant.

The inverters of the delay elements preferably contain current mirrors by means of which the driver currents in each case can be limited with no problem.

In accordance with one preferred embodiment the inverters each contain a p-type MOS field-effect transistor and an n-type MOS field-effect transistor, connected in series with a switching transistor. In this arrangement the delay of the individual delay elements can be usefully defined by the channel length of the current mirror transistors defining the driver current.

Although phase comparators of the kind as stated in the preamble of claim 15 are already known, these are, however, employed as a rule in conjunction with voltage-controlled oscillators. Using these conventional phase comparators in a digital clock generator is hampered by a series of drawbacks, for instance, their up and down outputs also being regularly activated at the same time, resulting particularly in the activation of a digital up-down counter at least being rendered difficult.

By contrast the digital phase comparator according to the invention which can be employed in particular in a digital clock generator contains means to lock the non-activated output in its non-activated status as long as the other output is being reset.

As a result of this configuration, activating a digital up-down counter in particular is substantially simplified, it being for instance sufficient for this purpose to output the digital phase comparator by a simple RS flip-flop, the set and reset inputs of which are to be connected to the two outputs of the digital phase comparator. This output RS flip-flop then furnishes at one output a single activating signal which preferably serves to activate the digital up-down counter of the clock generator according to the invention, via which the delay chain serving as an adjustable oscillator is controlled.

It is basically so, however, that one such digital phase comparator according to the invention can also be employed in conjunction with a voltage-controlled oscillator.

Further advantageous embodiments of the invention can be read from the subclaims.

The invention will now be explained in more detail on the basis of the example embodiments with reference to the drawing in which:

- Fig. 1 is a block diagram of a digital clock generator according to the invention,
- Fig. 2 is a schematic representation of the digital delay chain of the clock generator in its reset status,
- Fig. 3 illustrates the delay chain shown in Fig 2 directly following a change in status at its output,
- Fig. 4 is the circuit diagram of a delay chain element of the first kind,
- Fig. 5 is the circuit diagram of a delay chain element of the second kind,
- Fig. 6 is the circuit diagram of a known digital phase comparator,
- Fig. 7 illustrates the time profile of the signal at the inputs and outputs of the known phase comparator shown in Fig. 7,
- Fig. 8 is the circuit diagram of a digital phase comparator according to the invention, and
- Fig. 9 illustrates the time profile of the signal at the inputs and outputs of the known phase comparator shown in Fig. 8.

The embodiment of the digital clock generator according to the invention as shown in Fig. 1 contains a reference oscillator 10, an adjustable ring oscillator in the form of a digital closed digital chain 12, a digital programmable frequency divider 14 and a digital phase comparator 16.

The digital programmable frequency divider 14 is connected between the output of the delay chain 12 and one input of the phase comparator 16. The output of the reference oscillator 10 is connected to a further input of the phase comparator 16. The up-down counter 18 is connected to the output of the phase comparator 16. The output of this up-down counter 18 is connected at the one end to the delay chain 12 and, at the other, to an interpolation logic circuit 20, by means of which the delay chain 12 can be activated just the same as via the output of the up-down counter 18 as indicated by the arrows entered in the Fig.

The interpolation logic 20 assigned to the delay chain 12 contains a dual counter 22 which is clocked by the output signal of the delay chain 12. The count of the dual counter 22 is combined with the value of a number of least-significant bits of the output signal of the up-down counter 18 so that the number of changes in the length of the chain is defined by one step each for one corresponding clock cycle as a function of the value of the least-significant bits. The remaining most significant bits of the up-down counter 18 serve to address the delay chain directly by means as described in more detail below.

The output clock signal T_A furnishing the set frequency is fed back via the digital frequency divider 14 to the input V_2 of the phase comparator 16. Apart from the interpolation logic 20 thus output clock signal T_A is also preferably used to clock the up-down counter 18.

In the embodiment illustrated the reference oscillator 10 contains a 32 kHz oscillator quartz crystal. The output clock signal T_A is divided by the number 32 by the frequency divider 14. The delay chain 12 is composed of 32 weighted delay elements 24, 26 connected in series (viz. also Figs. 2 thru 5).

The up-down counter 18 is a 10-bit counter whilst the dual counter 22 used for the interpolation logic 20 is a 5-bit counter. The five least-significant bits of the output signal of the up-down counter 18 are combined accordingly with the count of the dual counter 22, whereas the five most-significant bits of the output signal of the up-down counter 18 are used to directly address the delay chain 12.

In the phase comparator 16 of the first-order system illustrated the output signal V_1 of the reference oscillator 10 is compared to the output signal V_2 of the programmable frequency divider 14 preset to the

divisor 32. In accordance with the result of this comparison the phase comparator 16 furnishes an output signal, by means of which the counting direction of the up-down counter 18 is determined. In accordance with the count of the up-down counter 18 and the control variable additionally furnished by the interpolation logic 20 the delay chain 12 is adjusted as regards its length so that the frequency deviation established by the phase comparator 16 is zero. When the frequency divider 14 is preset to the divisor 32 a freqiuency of 1 MHz thus results for the output clock signal T_A.

Figs. 2 and 3 are simple schematic representations of the digital closed delay chain 12 containing delay elements 24 alternately of the first kind, the outputs of which when reset (viz. Fig. 2) have the logic value 0, and delay elements 26 of a second kind, the outputs of which when reset have the logic value 1 In these Figs 2 and 3 each resulting output value of the delay elements 24, 26 in the reset condition is indicated by inverted commas.

Fig. 2 shows the status of the delay elements 24, 26 directly after resetting, whereby the status of the output at the end of the reset path 44 has just changed to the value 0 whilst this value also being applied at the same time to the input of the forward path 46 is still to cause a change in the status at the output of the first inverter of this forward path 46. Along the forward path 46 the inverters involved thus have the output values 0, 1, 0, 1, ...one after the other in the forward direction.

Corresponding values exist at the output of the inverters in the return path 44 when considering the sequence of values contrary to the direction of the run or, to put it otherwise, every delay element 24, 26 has an output in the forward direction and an output in the reverse direction, whereby the two outputs of the first delay element 24 (shown on the left in Fig. 2) have the value 0, the second delay element 26 has the output values 1, the third delay element 24 again having the output values 0, and so on.

Following each inverter 28, 30 of the forward path 46 and the return path 44 respectively an inverter 22 in the form of a ladder rung is connected between the forward path 46 and the return path 44. Via this transverse inverter 32 the length of the delay chain 12 can be shortened or lengthened by ways and means as described in more detail below. In this arrangement only one inverter 32 at a time is activated, upon which the remainder of the delay chain 12 (shown on the right in Figs. 2 and 3) in each case is no longer active.

Fig. 3 shows the status of the delay chain 12 immediately after the output of the delay chain 12 has changed its values from 0 to 1 and after the complete chain as shown in Fig.3 has been activated. Accordingly the outputs of the inverters in the forward path 46 and the return path 44 alternatively have the values 1, 0, 1, 0 and so on. In the illustration shown in Fig. 3 the value 1 at the output is still to affect the input of the first inverter of the forward path 46 and thus its output is still 1. By selecting an inverter 32 oriented transversely the chain can be suitably shortened, causing the frequency to be increased accordingly.

In Fig. 4 the circuit diagram of a delay element 24 of the first kind is shown which in the reset condition has the value 0 at the two outputs V_A and R_A.

By contrast Fig. 5 shows a delay element 26 of the second kind, the two outputs V_A and R_A of which have the value 0 in the reset condition.

Each of the delay elements 24, 26 alternately of the first and second kind in the delay chain 12 is assigned a forward inverter 28 and a return inverter 30 as well as a loop inverter 32 which when activated allows the corresponding length of the chain to be adjusted. The delay elements 24, 26 further contain two control inputs E, N via each of which their forward inverter 28 and return inverter 30 or their loop inverter 32 can be activated or the corresponding delay element 24, 26 reset. In this arrangement, addressing the delay chain 12 via the control inputs E, N is such that only one single loop inverter 32 at a time is activated. On top of this, resetting the delay elements 24, 26 is best done automatically on every power up.

In the delay element 24 of the first kind as shown in Fig. 4 the forward inverter contains a NOR gate 28 with the forward output V_A. The return inverter 30 with the return output R_A has an inverted control input IS via which it can be activated when a control signal 0 is applied. The loop inverter contains a NOR gate 32, the output of which is connected to the output R_A of the return inverter 30. This NOR gate 32 has a non-inverted control input NS via which it can be activated by an applied control signal 0. The forward input V_E of the delay element 24 is connected to an input of the NOR gate 32 and to an input of the NOR gate 28. One other input of the NOR gate 32 is connected to the output of an AND gate 48, the two inputs of which are connected to the control input E and the control input N respectively of the the delay element 24. The control input E is connected to yet a further input of the NOR gate 28. On top of this, the other control input E is connected to both the inverting control input IS of the return inverter 30 and to the non-inverting control input NS of the NOR gate 32.

The function of this delay element 24 of the first kind is evident from the following truth table:

E	N	V_A	R_A
0	1	^-V_E	^-R_E
1	0	0	^-V_E
1	1	0	0

Table 1

indicating that the two outputs V_A and R_A of the delay element 24 are reset to the value 0 when both control inputs E, N have the value 1.

When, on the other hand, the control input E assumes the value 0 and the control input N the value 1, then the forward inverter 28 and the return inverter 30 are activated whilst the loop inverter 32 is deactivated. Accordingly, the inverted value ^-V_E of the forward input V_E appears at the forward output V_A whilst at the reference oscillator R_A the inverted value ^-R_E appears at the return input R_E.

The loop inverter 32 is then activated or addressed when the control input W has the value 1 and the control input N the value 0. In this case the value of the forward output V_A equals 0 whilst the reference oscillator R_A equals the inverted value ^-V_E of the forward input V_E. In this case the length of the delay chain 12 is determined by this loop inverter 32. The remaining loop inverter remains deactivated.

In the delay element 26 of the second kind shown in Fig. 5 the forward input 28 contans a NAND gate 28 and the loop inverter a NAND gate 32. An inverting control input IS of the NAND gate 28 is connected together with a non-inverting control input NS of the return input 30 to the control input N of the delay element 26. This control input N is further connected to an input of the NAND gate 28 and to an input of an OR gate 50 which has a further input connected to the control input E of the delay element 26. The output of the OR gate 50 is connected to an input of the NAND gate 32 which has a further input to which the forward input V_E of the delay element 26 is connected. At this forward input V_E of the delay element 26 a further input of the NAND gate 28 is connected. The forward output V_A is formed by the output of this NAND gate 28. The output of the return input 30 and the output of the NAND gate 32 are connected to the reference oscillator R_A of the delay element 26 whilst the return input R_E of the delay element 26 is formed by the input of the return input 30.

The function of this delay element 26 of the second kind is evident from the following truth table:

E	N	V_A	R_A
0	1	^-V_E	^-R_E
1	0	1	^-V_E
0	0	1	1

Table 2

indicating that each of the two outputs V_A and R_A of the delay element 26 are reset to the value 1 when both control inputs E, N have the value 1.

When the control input E is set to the value 0 and the control input N to the value 1, then the forward inverter 28 and the return inverter 30 are activated whilst the loop inverter 32 remains deactivated. In this case the inverted value ^-V_E of the forward input V_E results at the forward output V_A and the inverted value ^-R_E of the return input R_E at the reference oscillator R_E.

If, however, the control input E assumes the value 1 and the control input N the value 0, the loop inverter 32 is activated, resulting in the inverted value ^-V_E of the forward input V_E occurring at the return input R_A whilst the forward output V_A is held at the value 1.

As evident from Figs. 2 and 3 the delay chain 12 has a delay element 24 of the first kind at the end furnishing the output clock signal T_A.

Achieving the transistor circuitry of this delay chain 12 deviates somewhat from the usual CMOS structure. All inverters 28, 30, 32 contain current mirror circuits to limit the driver current in each case. A bias voltage generator furnishes the voltage for gating a p-type MOS FET and an n-type MOS FET connected in series with the switching transistors. Accordingly, the output current of each delay element 24, 26 can easily be determined by the channel length ratios. The width of all transistors and the length of the switching transistors can be reduced to a minimum. To reduce the switching noise between the stages and to avoid charge takeover effects the current mirror transistors can be directly connected to the output.

The current consumption within the delay chain 12 is mainly determined by the capacitances between the delay elements 24, 26 needing to be repoled.

The setpoint frequency of 1 MHz should be attained under normal conditions (3 V, 27 °C typical fabrication parameters) by roughly half of the delay chain 12 being activated, this leaving enough space to both ends for deviations from the nominal values. A capacitance of 2 x 70 fF is achieved for each delay element, for instance, as long as the circuit has been designed for a minimum capacitance. The current needed to repole 32 capacitances of 16 delay elements 24, 26 is given by the following:

$$I = \frac{32 \times 70\ fF \times 1.5\ V}{0.5\ \mu s} \approx 7\mu A$$

The maximum step in frequency from one delay element 24, 26 to the next should not exceed 1/6. Accordingly the delay chain 12 should preferably contain at least six delay elements 24, 26.

The delay of the various delay elements 24, 26 can be increased with increasing length of the chain without the step in frequency being greater than 1/6. For example, the 13th delay element can have twice the delay than that of the first delay element.

The delay of the various delay elements can simply be increased by correspondingly increasing the channel length of the transistors defining the current in the current mirror concerned. In this way the percentual change in the frequency from one delay element to the next can be maintained more or less constant, whereby the usual deviations in the fabrication parameters are tolerable.

The first 9 delay elements 24, 26 can furnish a driver current of approx. 10 µA, the maximum output then being continually reduced. For setpoint frequencies other than 1 MHz the repoling current can be simply changed, for example, by changing the resistor determining the current in the bias voltage generator.

A conventional CMOS inverter may be employed at least as a loop inverter.

Every change in the addressing of the delay chain 12 or the length thereof requires a corresponding change in the values of both control inputs E, N. Since it cannot be assured in general that both control signals change at the same time and thus a reset condition can materialize for a brief instant, the change in the address should be effective at the moment the status as shown in Fig. 2 occurs so that no signal spikes are produced whatsoever even if there is a fleeting occurrence of the reset mode.

The frequency divider 14, the interpolation logic circuit 20 and the up-down counter are clocked with the output of the delay chain 12. This clock pulse, having a frequency of 1 MHz for instance, is divided, by the frequency divider 14 by, for example,32 and compared to the 32 kHz reference frequency in the phase comparator 16. The frequency divider 14 is programmable, for example, between 1 and 127.

The output signal of the phase comparator 16 then dictates the counting direction of the 10 bit up-down counter 18, the five most-significant bits of which directly address the delay chain 12.

It must be assured that the return edge of the clock pulse in the chain does not attain the loop or turning point before the change in the address. The maximum adjustable frequency is normally limited by the delays of the frequency divider 14, the phase comparator 16, the interpolation logic circuit 20 and the 10 bit up-down counter 18. This loop (turning) point is attained after 1/4 of the clock cycle.

If the delay is excessive, this could easily give rise to a noisy signal spike. This problem can be remedied right from the start by locking the address directly following the rising edge of the clock pulse. Sufficient time is then available (half a clock cycle) to establish the new address, since the locking circuit at the input of the delay chain does not again become transparent until the falling edge of the clock pulse occurs. A fleeting occurrence of the reset mode at this point in time can no longer cause a signal spike as is clearly evident from Fig. 2.

In case a reset mode occurs the outputs of a corresponding delay chain 24 of the first kind are set to 0, whilst the outputs of a corresponding delay chain 26 of the second kind are set to 1.

Since for a frequency divider 14 preset e.g. to 32 the counting direction of the 10 bit up-down counter 18 can be changed at best not before 32 clock pulses, when new information is present at the output of the phase comparator 16, it is likely that in the frequency-locked condition the up-down counter 18 will count in the wrong direction for various clock cycles. Expressed otherwise, the frequency can swing about the locked value. Even after 32 clock cycles the counting direction cannot be instantly sensed. Since the actual frequency and the setpoint frequency are not far apart, several 32 kHz clock cycles may be necessary to establish the deviation in frequency.

To improve the response of the clock generator the five most-significant bits of the up-down counter 18 are used to address the delay chain 12, whilst the remaining five least-significant bits are combined with the outputs of the 5-bit dual counter 22 of the interpolation logic circuit 20. The higher the value of the five least-significant bits, the more often is the delay chain 12 shortened by one step for a clock cycle. Using this 5-bit dual counter 22 ensures that shortening of the chain occurs in the same time frame.

The following Table indicates when the delay chain 12 is shortened by one step each time, whereby the output value of the 5-bit dual counter 22 is given in the horizontal direction and the value of the five least-significant bits of the 10 bit up-down counter is given in the vertical direction.

	0	1/ 17	2/ 18	3/ 19	4/ 20	5/ 21	6/ 22	7/ 23	8/ 24	9/ 25	10 26	11 27	12 28	13 29	14 30	15 31	16
0																	
1																	x
2									x								
3									x								x
4					x								x				
5					x								x				x
6					x				x				x				
7					x				x				x				x
8			x				x				x				x		
9			x				x				x				x		x
10			x				x		x		x				x		
11			x				x		x		x				x		x
12			x		x		x				x		x		x		
13			x		x		x				x		x		x		x
14			x		x		x		x		x		x		x		
15			x		x		x		x		x		x		x		x
16		x		x		x		x		x		x		x		x	
17		x		x		x		x		x		x		x		x	x
18		x		x		x		x	x	x		x		x		x	
19		x		x		x		x	x	x		x		x		x	x
20		x		x	x	x		x		x		x	x	x		x	
21		x		x	x	x		x		x		x	x	x		x	x
22		x		x	x	x		x	x	x		x	x	x		x	
23		x		x	x	x		x	x	x		x	x	x		x	x
24		x	x	x		x	x	x		x	x	x		x	x	x	
25		x	x	x		x	x	x		x	x	x		x	x	x	x
26		x	x	x		x	x	x	x	x	x	x		x	x	x	
27		x	x	x		x	x	x	x	x	x	x		x	x	x	x
28		x	x	x	x	x	x	x		x	x	x	x	x	x	x	
29		x	x	x	x	x	x	x		x	x	x	x	x	x	x	x
30		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
31		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

(Table 2)

After this the step change frequency with the value of the five least-significant bits of the up-down counter 18 increases.

This interpolation logic 20 supports elevating the control frequency in the locked status so that the frequency deviation as a whole is reduced within brief periods of time.

The phase generator 16 of the clock generator shown in Fig. 1 serves to define the counting direction of the up-down counter 18 in the all-digital loop.This up-down counter furnishes a corresponding output signal, by means of which the length of the closed delay chain 12 and thus the setpoint frequency is controlled.

The digital phase comparator used for this purpose may have, for example, an up output and a down output to establish the counting direction of the up-down counter 18 according to the status of the two input signals V_1, V_2 (viz. Fig. 1). In this respect the digital phase comparator can be suitably designed so that, depending on which of the two input signals first assumes its active value, the assigned up output and down

output respectively is set to an active value and reset following the other input signal becoming active. Phase comparators of this kind are already employed in PLL circuits in which the duty cycle of both outputs is employed as a measure of the deviation in phase and frequency.

Such a phase comparator cannot, however, be employed directly in the digital clock generator shown in Fig. 1, especially since to activate the up-down counter 18 a discrete control signal is to be preferably provided, by means of which the corresponding counting direction is determined. One simple solution of creating such a discrete control signal could be to connect the up and down outputs of the digital phase comparator to the set and reset inputs of a discrete RS flip-flop and to pick off the control signal at one output of this flip-flop. However, this solution may result in noisy voltage spikes when using known digital phase comparators as is evident from Figs. 6 and 7.

In Fig. 6 a known digital phase comparator is shown having two inputs for the input signals V_1 and V_2 and an up output 34 and a down output 36.

The inputs V_1 and V_2 of this known digital phase comparator simultaneously form the inputs of two input gates, i.e. NAND gate 52 and NAND gate 54 respectively. On the one hand the output of the NAND gate 52 is connected to the set input S of an RS flip-flop 56 comprising two NAND gates 56', 56'' and, on the other, to an input of an output gate, namely the NAND gate 60. The output of the NAND gate 60 is fed back to a further input of the NAND gate 52. The output of the NAND gate 60 forms simultaneously the up output 34 of the digital phase comparator.

Correspondingly, the output of the NAND gate 54 is connected on the one hand to the set input S of an RS flip-flop 58 comprising two NAND gates 58', 58'' and, on the other, to an input of an output gate, namely the NAND gate 62. In turn, the output of the NAND gate 62 is fed back to a further input of the NAND gate 54, the output of the NAND gate 62 forms simultaneously the down output 36 of the digital phase comparator.

The output Q of the RS flip-flop 56 is connected on the one hand to a further input of the NAND gate 60 and, on the other, to an input of a further NAND gate 64. The output Q of the other RS flip-flop 58 is connected on the one hand to a further input of the NAND gate 62 and, on the other, to a further input of NAND gate 64. This NAND gate 64 has two further inputs which are connected to the output of the NAND gate 52 and the output of the NAND gate 54 respectively. The output of the NAND gate 64 is connected to a third input of the NAND gate 60 as well as to a third input of the NAND gate 62 and, in addition to this, is also connected to the reset input R of the RS flip-flop 56 as well as to the corresponding reset input R of the RS flip-flop 58.

In this known digital phase comparator the NAND gate 64 accordingly serves to reset the up and down outputs 34, 36 of the phase comparator to 1 and the two RS flip-flops 56, 58 to 0.

Otherwise the functioning of this known phase comparator is evident from the time signal profiles as shown in Fig. 7 to which reference is made in the following.

When - for $V_1 = 0$ and $V_2 = 0$ - the two RS flip-flops 56, 58 are reset to the value 0, then the two up and down outputs 34, 36 of the digital phase comparator are each reset to 1. If then the input signal $V_1 = 1$ the RS flip-flop 56 is set to the value 1. The up and down outputs 34, 36 of the phase comparator continue to have the value 1.

Should then the other input signal V_2 assume the value 1, then the other RS flip-flop 58 will additionally be set to 1. The up and down outputs 34, 36 of the digital phase comparator continue to have the value 1. By the next falling edge of the of the input signal V_1 or of the input signal V_2 the corresponding output 34 and 36 respectively of the phase comparator is set to the active value 0.

When we now assume, for example, that input signal V_1 is the first to reassume the value 0, then the up output 34 of the phase comparator will be accordingly set to active 0. The down output 36 retains its value 1.

When subsequently the input signal V_2 also reassumes the value 0 the up output 34 is reset, as wanted, to the value 1, but at the same time an unwanted 0 pulse (viz. Fig. 7) materializes at the down output 36 which can result in pulse signal noise when the up counter 18 (Fig. 1) is activated. In particular it is directly not possible to generate a single activation signal for the up-down counter 18 by providing one further RS flip-flop at the output. In this case too, there is no assurance of the circuit being free of noise.

If, instead however, the input signal V_2 assumes the value 0, then the down output 36 will first be set to the value 0. If then the input signal V_1 also reassumes the value 0, the down output 36 previously set to 0 will be reset to 1. In this case, however, a noisy 0 pulse results at the up output 34 (viz. Fig. 7).

Now in turning to Fig. 8 an embodiment of the digital phase comparator according to the invention will be evident which can be used to advantage particularly in the clock generator according to the invention as shown in Fig. 1.

This digital phase comparator according to the invention comprises in turn two input gates, namely NAND gate 52 and NAND gate 54. The input signal V_1 is applied to one input of the NAND gate 52 whilst the other input signal V_2 is available at one input of the NAND gate 54.

The output of the NAND gate 52 is connected on the one hand to the set input ^{-}S of an RS flip-flop 56 comprising two NAND gates 56', 56'' and, on the other, to one input of an output gate, namely NAND gate 60. The output Q of the RS flip-flop 56 is connected to a further input of the NAND gate 60. The output of the NAND gate 60 connected to the up output 34 of the digital phase comparator is fed back to a further input of the NAND gate 52.

The output of the NAND gate 54 is connected on the one hand to the set input ^{-}S of an RS flip-flop 58 and, on the other, to one input of an output gate, namely NAND gate 62. The output Q of the RS flip-flop 58 is connected to a further input of the NAND gate 62. The output of the NAND gate 62 forming the down output 36 of the digital phase comparator is fed back to a further input of the NAND gate 54.

To this extent this digital phase comparator is identical to the one shown in Fig. 6 and thus like reference numerals are used for like gates.

In the phase comparator according to the invention as shown in Fig. 8, however, the function of the NAND gate 64 provided in the known phase comparator (viz. Fig. 6) is shared by three NAND gates 40, 42, 68 and a NOR gate 66. In addition a further reset input RÜCK is provided to return the circuit to a defined status preferably on power up. An embodiment of one such configuration of the digital phase comparator according to the invention will now be evident from the following description, again with reference to Fig. 8.

With reference thereto output Q of the RS flip-flop 56 is additionally connected to an input of a NAND gate 40, the output of which is connected to a further input of the NAND gate 62.

Accordingly output Q of the RS flip-flop 58 is additionally connected to an output of a NAND gate 42. the output of which is connected to a further input of the NAND gate 60.

One further input of the NAND gate 40 is connected to the output of the NAND gate 52 whilst a further input of the NAND gate 42 is connected to the output of the NAND gate 54.

The output ^{-}Q of the RS flip-flop 56 is connected to an input of a NOR gate 66 having a further input to which the corresponding output ^{-}Q of the RS flip-flop 58 is connected. The output of the NOR gate 66 is connected to one input of a further NAND gate 68 having two further inputs which are connected to the output of the NAND gate 52 and the output of the NAND gate 54 respectively. The output of the NAND gate 68 is simultanously connected to both one reset input ^{-}R of the RS flip-flop 56 and one reset input ^{-}R of the RS flip-flop 58.

On top of this the digital phase comparator according to the invention is provided with an additional reset input RÜCK which is connected to a further reset input R of the RS flip-flop 56, a further reset input ^{-}R of the RS flip-flop 58, a further input of the NAND gate 52 as well as to a further input of the NAND gate 54.

The way in which the digital phase comparator according to the invention functions will now be evident from considering the time signal profiles shown in Fig. 9 illustrating the two input signals V1, V2 as well as the output signals at the down and up outputs 34, 36 as a function of time.

When both input signals V_1, V_2 are each 0 and both RS flip-flops 56, 58 are reset to 0 (output Q) the up and down outputs 34, 36 of the digital phase comparator according to the invention are reset to 1. In this defined output status the phase comparator can be set in particular by a 0 pulse at the additional reset input RÜCK.

When the input signal V_1 additionally assumes the value 1, the assigned RS flip-flop 56 is set to the value 1 (output Q).

When the input signal V_2 then assumes the value 1, the further RS flip-flop 58 will also be set to the value 1 (output Q) whereby the output of the NOR gate 66 changes in value from 0 to 1 since both the output ^{-}Q of the RS flip-flop 56 as well as the output ^{-}Q of the RS flip-flop 58 each assume the value 0.

If the input signal V_1 is then the first to change its value from 1 to 0 again, then active 0 is set accordingly at the up output 34. Here, the important thing is that due to the change in the input signal V_1 the output of the NAND gate 40 is also set to the value 0.

When the other input signal V_2 also reassumes the value 0, RS flip-flop 58 is first reset to the value 0 (output Q). With value 1 at the output of the NAND gate 54 the value 0 will also occur at first at the output of the NAND gate 68, this also causing the other RS flip-flop 56 to be reset to the value 0 (output Q). Accordingly the up output 34 of the digital phase comparator is reset to the value 1. Since the NAND gate 40 first maintains the value 0 at its output, until also the RS flip-flop 56 has been reset to 0 (output Q) and, before then, the output Q of the RS flip-flop 58 has already been set to the value 0, the down output 36 of the digital phase comparator is maintained (locked) to its existing value 1 at the same time as the up output 34 is reset to the value 1. When the output of the NAND gate 40 again assumes the value 1 after RS flip-

flop 56 has been reset, then as soon as the output Q of the RS flip-flop 58 assumes the value 0 it is already assured that the NAND gate 62 continues to retain the value 1 at the down output 36.

As soon as the RS flip-flop 58 has been reset, the value 0 materializes at the output of the NOR gate 66, this in turn causing the output of the NAND gate 68 to be reset to the value 1 so that the reset pulse at the output of this NAND gate 68 or at the reset inputs $\overline{R}$ of the two RS flip-flops 56,58 is terminated.

If, instead, the input signal V_2 is the first to assume the value 0, then the down output 36 of the digital phase comparator is first set to 0. Should then the input signal V_1 change to the value 0,then the down output 36 too will be reset to 0 without any negative pulse materializing at the up output 34. In this case the NAND gate 42 ensures that the value 1 is maintained or locked at the up output 34.

The fact that a pulse occurs at both the up output 34 and the down output 36 when the two input signals V1 and V2 are negative-going in coincidence is uncritical, since in this case there is no correct or incorrect counting direction.

As a result of this configuration it is thus assured an active 0 signal exists at only one of the two outputs 34, 36 at any one time. Now, however, a simple RS flip-flop 38 can be used in particular for generating a single activation signal for the up-down counter 18 (viz. Fig. 1) as is evident from Fig. 8. In this arrangement it is useful to connect the up output 34 to the set input S and the down output 36 to the reset input R of the RS flip-flop 38. An output Q of this RS flip-flop 38 then dictates the counting direction of the up-down counter 18 of the digital clock generator shown in Fig. 1.

The digital phase comparator according to the invention may be put to use, however,not only in all-digital loops such as in particular in the clock generator as shown in Fig. 1 but also, for example, in combination with an oscillator, e.g. in an analog loop.

In addition to this, instead of active 0 signals it is also possible to basically to use active 1 signals, for the purpose of which a correspondingly complementary circuit configuration is to be selected. Finally, instead of the RS flip-flop 38, any other suitable terminating circuit for generating the single activation signal for the digital up-down counter may be provided.

It is useful to reset the length of the delay chain 16 to its maximum value on power up, the phase comparator then preferably setting its up output to the active value until the frequency produced at the output of the frequency divider is more or less the same as the reference frequency.

Any shift in phase at the set frequency may be counteracted, for example, by reducing the extent of the switching stages in the delay chain and/or by by synchronizing the output signal of the frequency divider with the reference frequency as soon as the phase shift exceeds a critical value, thus enabling the amplitude of any oscillation about the set value (jitter) to be significantly reduced. Since fleeting deviations in frequency are also reduced to a minimum, exceptionally precise adjustment of frequency is possible so that even protocols of an asynchronous data exchange can be made use of.

Since the circuit permits programming, simple handling is assured. The control action can be simply defeated and discrete frequencies can be programmed as desired. Deactivating the closed control loop and selecting lower frequencies results in the current consumption of the complete system being further reduced.

Normally closed loop control commences on power up of the full chain length, i.e.at the lowest possible frequency.

The time need to set the delay chain can be further reduced, for example, by counting the clock pulses generated within one cycle of the reference frequency for the complete chain and calculating the setpoint length, thus enabling the chain to be preset to this calculated length so that the total time needed for adjustment after power up is reduced.

Claims

1. A clock generator having a reference oscillator (10), an adjustable oscillator (12), a frequency divider (14) and a phase comparator (16), said frequency divider (14) being connected between the output of said adjustable oscillator (12) and one input of said phase comparator (16), the output of said reference oscillator (10) being connected to a further input of said phase comparator (16) and the adjustment of said oscillator (12) depending on the output signal of said phase comparator (16) characterized in that said adjustable oscillator is a digital closed delay chain (12), said frequency divider is a digital programmable frequency divider (14) and in that between the output of said phase comparator (16) and said delay chain (12) a digital up-down counter (18) is connected, the counting direction of which is determined by the output signal of said phase comparator (16) and by means of which the corresponding length of said delay chain (12) is adjustable.

2. A clock generator as set forth in claim 1, characterized in that said delay chain (12) is assigned an interpolation logic (20) containing a dual counter (22) which is clocked by the output signal of said delay chain (12), the count of this dual counter being combined with the value of a number of least-significant bits of the output signal of said up-down counter (18) to define, as a function of the value of these least-significant bits. the number of changes in the length of said delay chain by one step at a time for each clock cycle whilst the remaining most-significant bits directly address said delay chain (12).

3. A clock generator as set forth in claim 1 or 2, characterized in that said delay chain (12) is composed of a plurality of delay elements (24, 26) connected in series, each containing a forward inverter (28), a return inverter (30) as well as a loop inverter (32), by the activation of which each length of said chain is adjustable.

4. A clock generator as set forth in claim 3, characterized in that said delay elements (24, 26) have control inputs (E, N) via which their forward inverters (28) and their return inverters (30) or their loop inverters (32) can be activated or the corresponding delay element (24, 26) can be reset.

5. A clock generator as set forth in claim 4, characterized in that the addressing of said delay chain (12) via said control inputs (E, N) is such that only one loop inverter (32) at a time is activated.

6. A clock generator as set forth in claim 3 thu 5, characterized in that said delay chain (12) has alternating delay elements (24) of a first kind, the outputs of which are logical 0 in the reset condition, and delay elements (26) of a second kind the outputs of which are logical 1 in the reset condition.

7. A clock generator as set forth in claim 6, characterized in that said delay elements (24, 26) are automatically reset on power up.

8. A clock generator as set forth in claim 6 or 7, characterized in that said delay chain (12) has a delay element (24) of the first kind at the end furnishing the output clock signal (T_A).

9. A clock generator as set forth in any of the claims 3 thru 8, characterized in that said delay chain (12) contains at least six delay elements (24, 26).

10. A clock generator as set forth in claims 3 thru 9, characterized in that said delay elements (24, 26) have at least in part a differing delay.

11. A clock generator as set forth in claim 10, characterized in that with increasing chain length the additional delay elements (24, 26) have a higher delay than the delay elements (24, 26) required for a shorter chain length.

12. A clock generator as set forth in claims 3 thru 11, characterized in that said inverters (28, 30, 32) contain current mirror circuits to limit the driver current in each case.

13. A clock generator as set forth in claims 3 thru 12, characterized in that said inverters (28, 30, 32) each contain a p-type MOS field-effect transistor and an n-type MOS field-effect transistor connected in series with a switching transistor.

14. A clock generator as set forth in claims 3 thru 13, characterized in that the delay of the individual delay elements (24, 26) is determined at least substantially by the channel length of the transistors of said current mirror circuits determining the driver current.

15. A digital phase comparator particularly for use in a clock generator according to any of the preceding claims having an up output (34) and a down output (36) to activate an adjustable oscillator (18) according to the status of two input signals (V_1, V_2) whereby depending on which of said two input signals (V_1, V_2) first assumes its active value (0), the assigned up output (34) and down output (36) respectively is set to an active value (0) and reset following the other input signal becoming active, characterized in that means (40, 42) are provided to lock the non-activated output (34, 36) during resetting of the other output (34, 36) in its non-activated status.

16. A digital phase comparator as set forth in claim 15, characterized in that said up and down outputs (34, 36) have an output RS flip-flop (38) and that said up and down outputs (34, 36) are connected to the set and reset inputs (S, R) of said output RS flip-flop (38), the latter (38) furnishing at an output (Q) a single activating signal for said adjustable oscillator (18).

17. A digital phase comparator as set forth in the claims 15 or 16, characterized in that said adjustable oscillator contains a digital closed delay chain (12) which is controlled by a digital up-down counter (18), the counting direction of which is assignable by said activation signal.

18. A digital phase comparator as set forth in claims 15 or 16, characterized in that said adjustable oscillator is a voltage-controlled oscillator.

FIG. 1

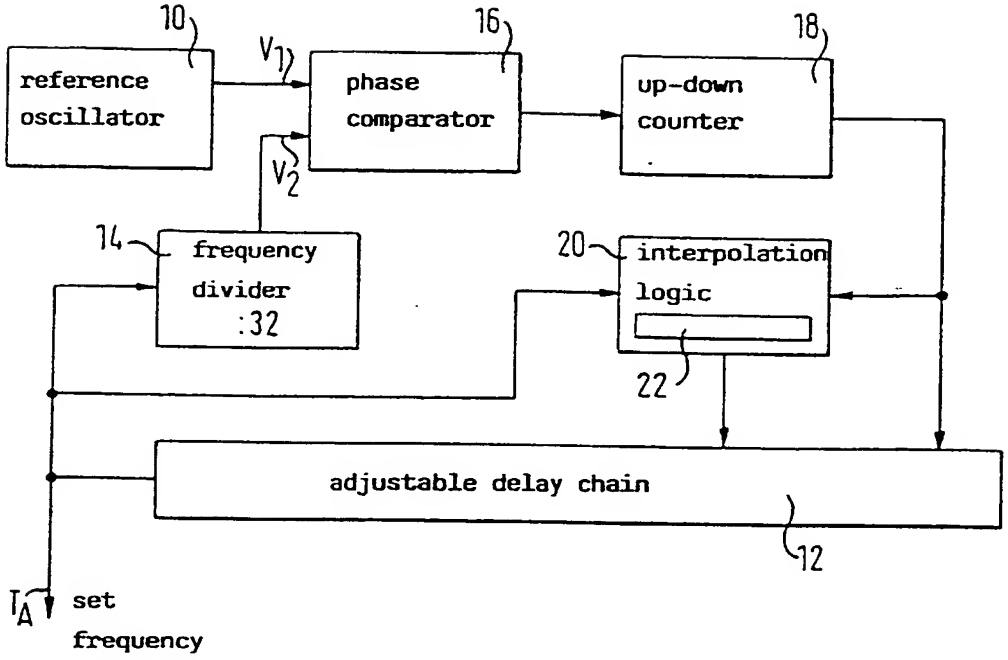


FIG. 2

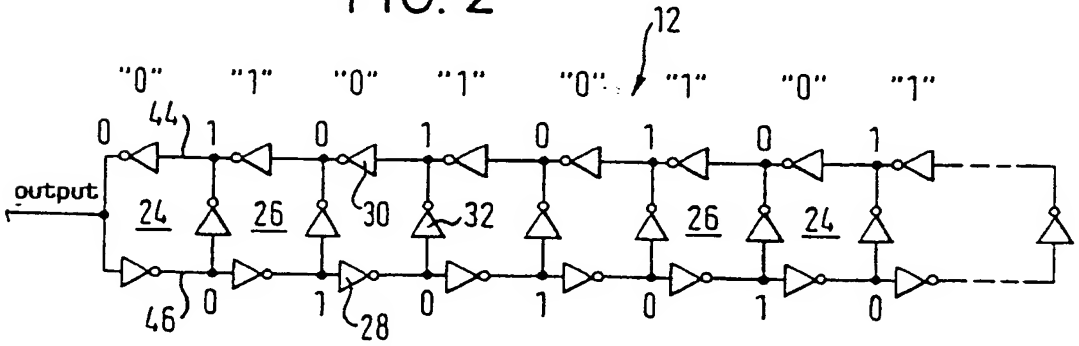


FIG. 3

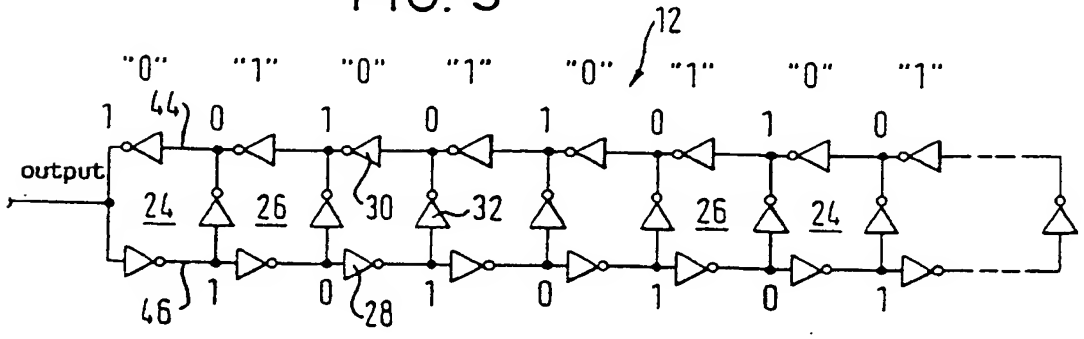


FIG. 4

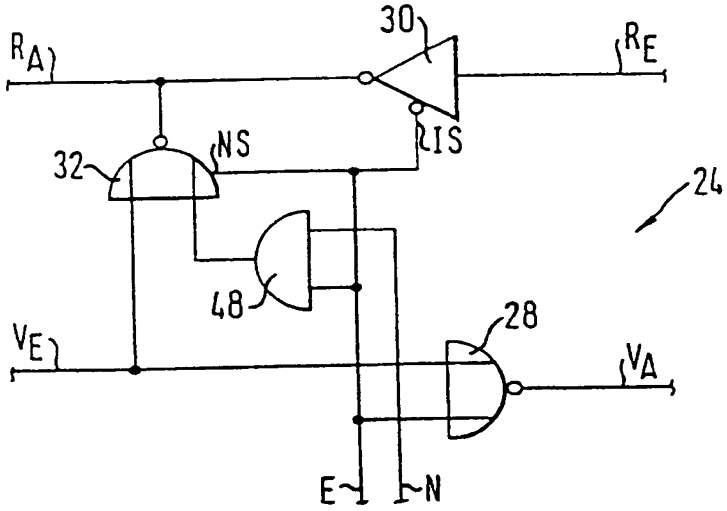


FIG. 5

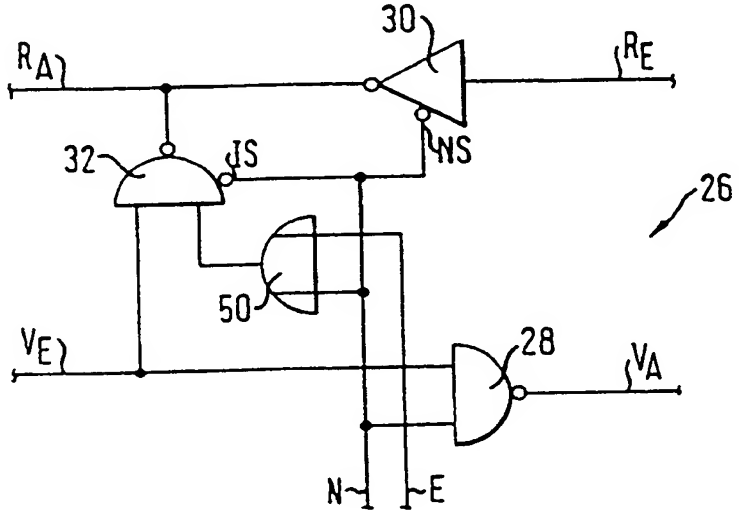


FIG. 6

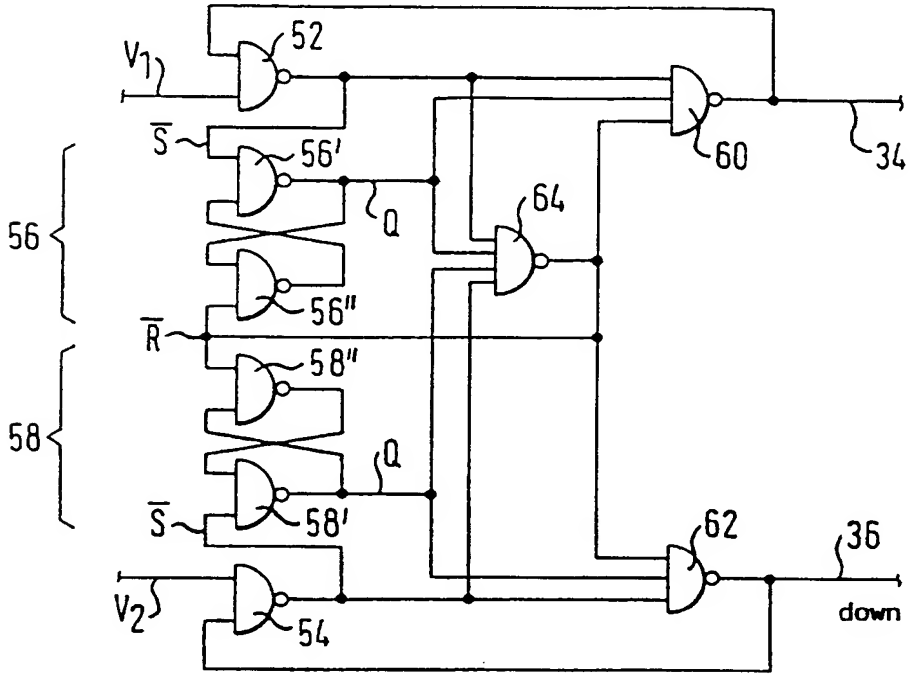

52
V_1
$\overline{S}$
56'
Q
56
56''
$\overline{R}$
58''
58
Q
$\overline{S}$
58'
V_2
54
64
60
34
62
36
down

FIG. 7

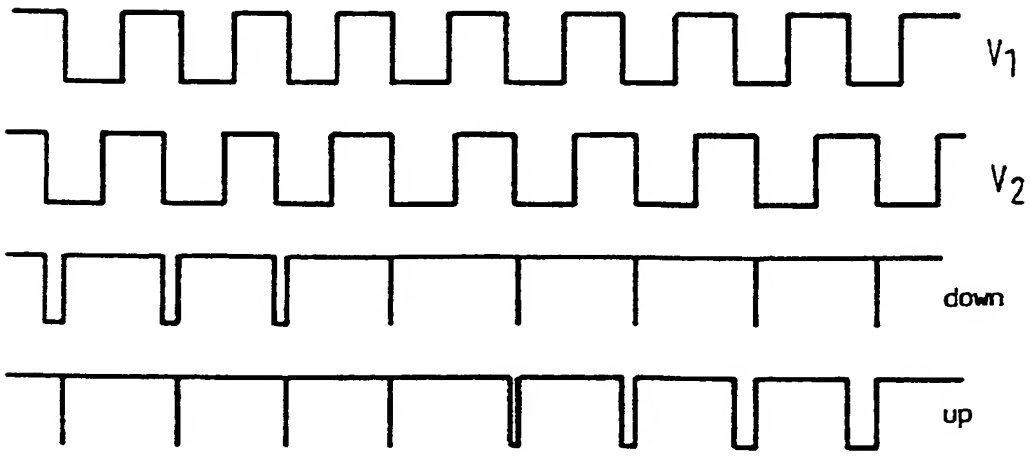

V_1
V_2
down
up

FIG. 8

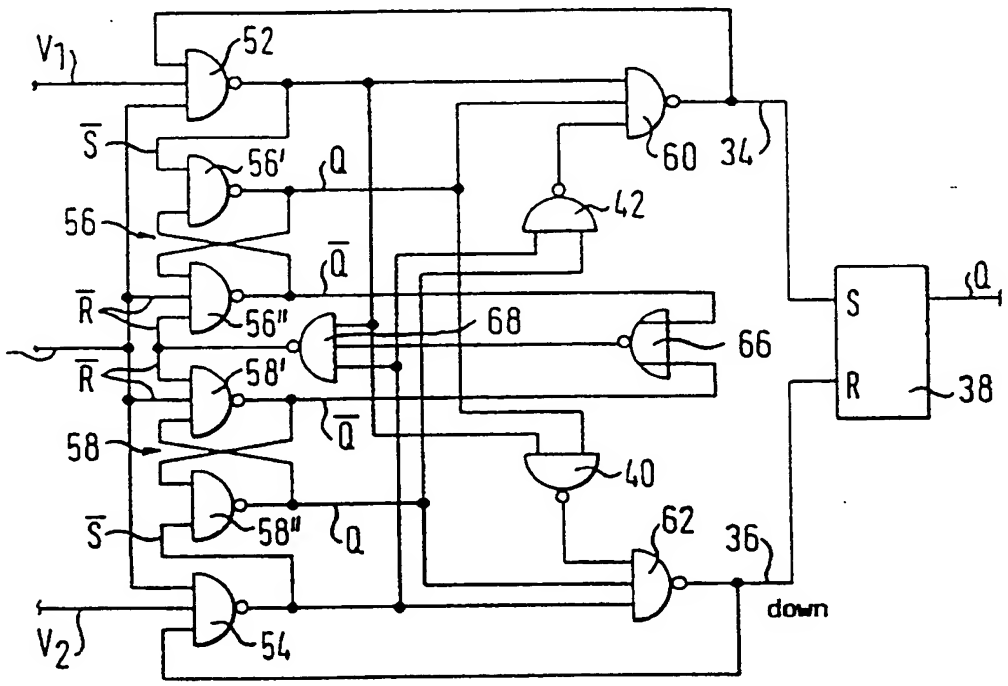

V1
52
S
56'
Q
56
Q
R
56"
68
66
R
58'
Q
58
40
S
58"
Q
62
36
down
V2
54
60
34
42
S
Q
R
38

FIG. 9

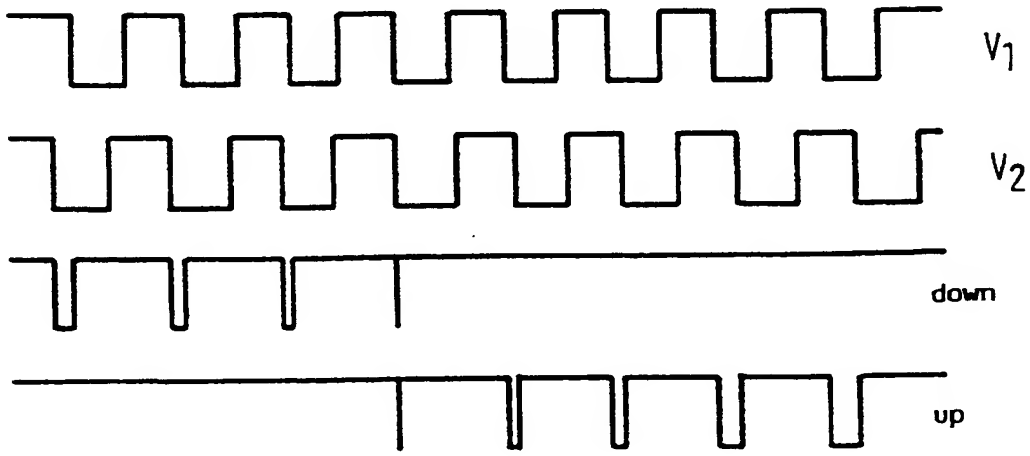

V1
V2
down
up

FIG. 1

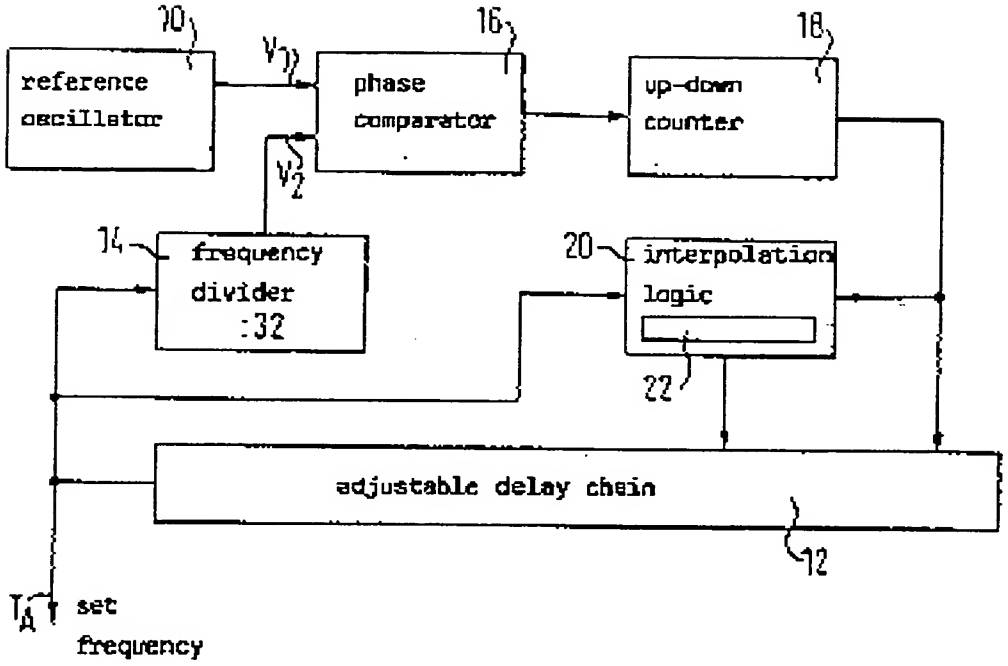


FIG. 2

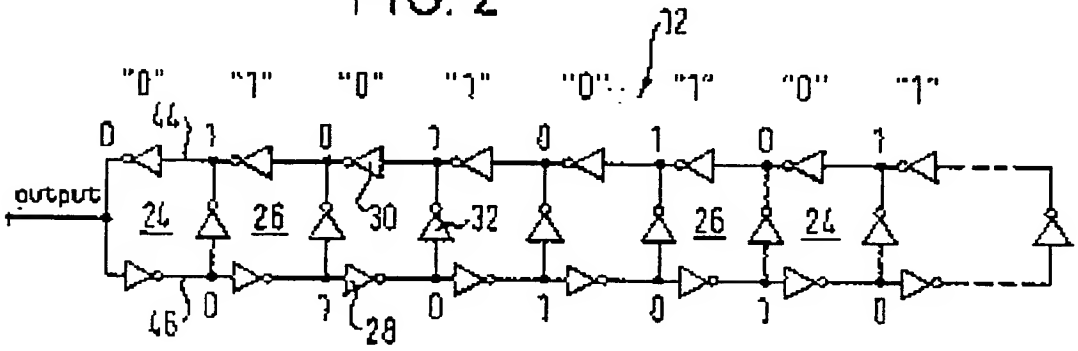


FIG. 3

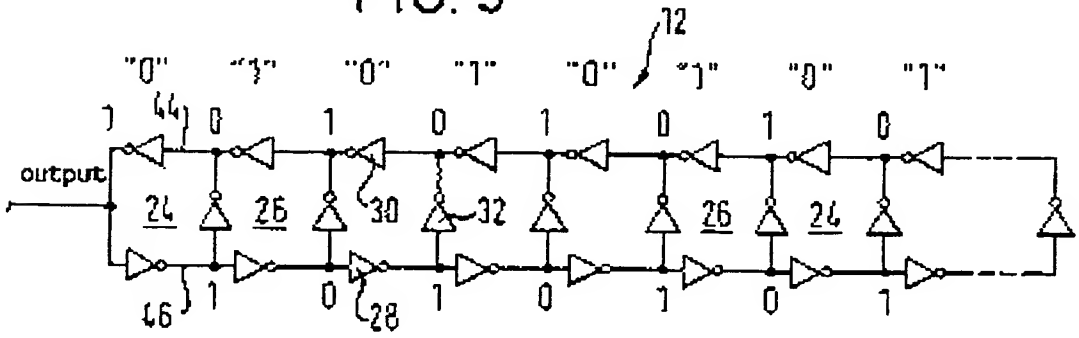


FIG. 4

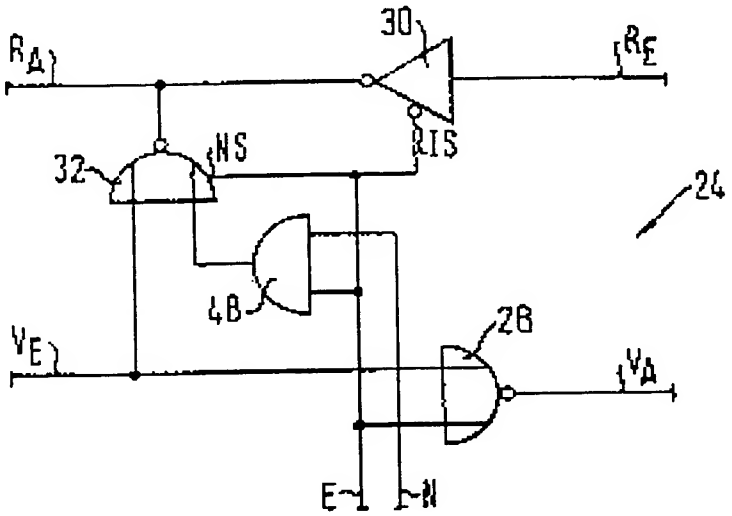


FIG. 5

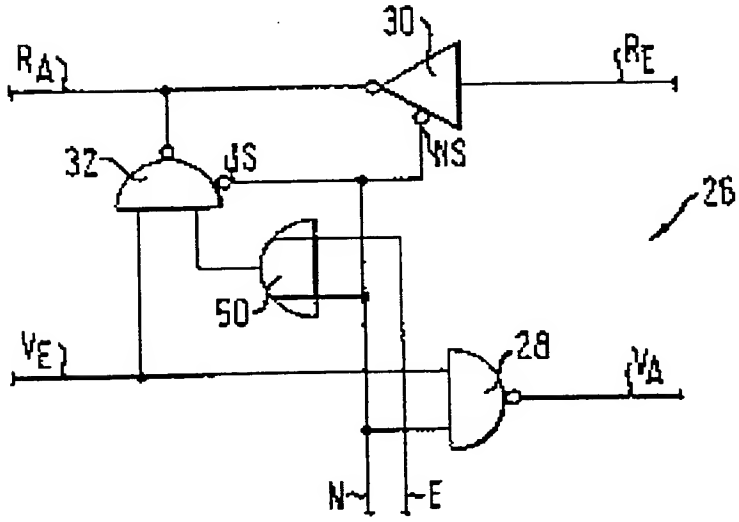


FIG. 6

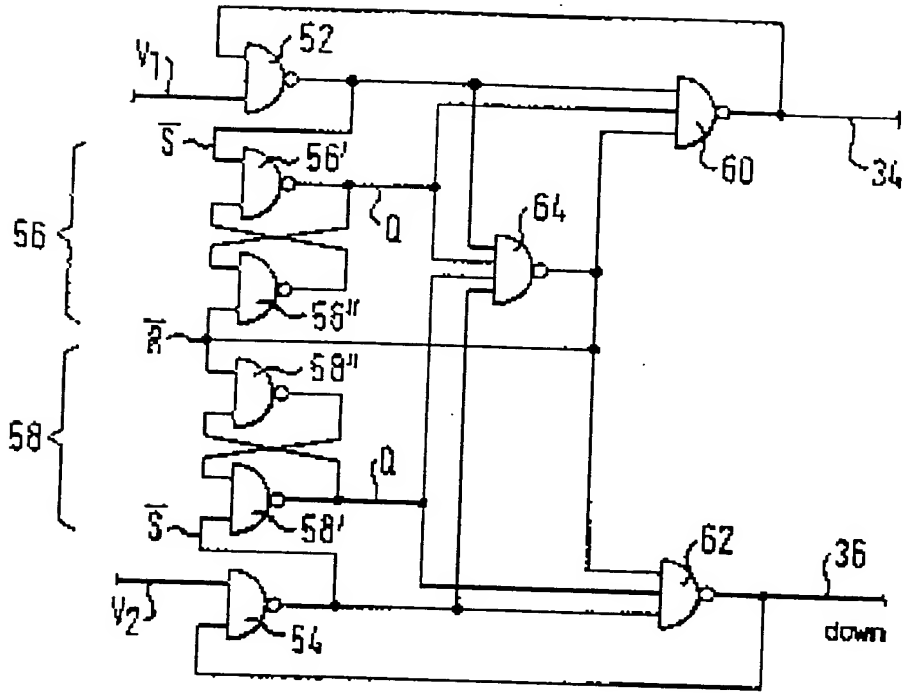

52
V_1
$\overline{S}$
56'
Q
56
56''
$\overline{R}$
58''
58
Q
$\overline{S}$
58'
V_2
54
64
60
34
62
36
down

FIG. 7

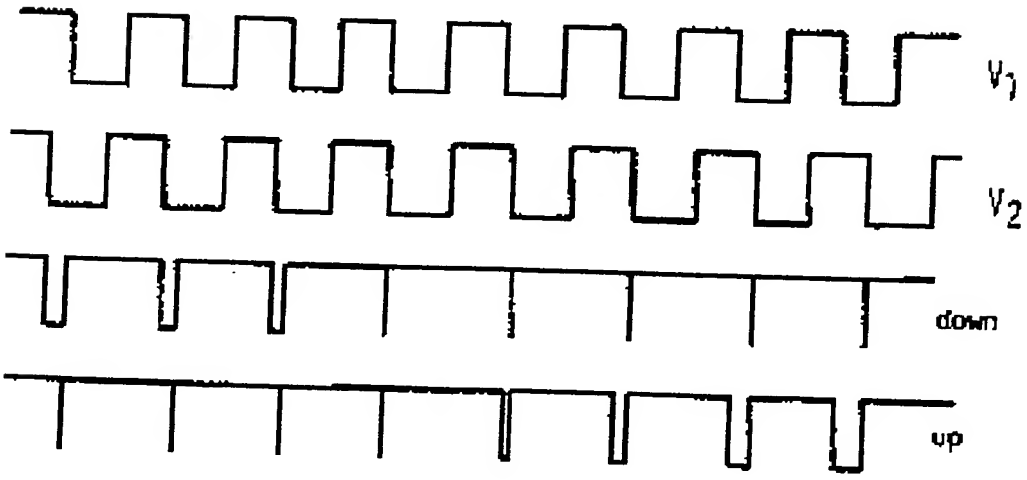

V_1
V_2
down
up

FIG. 8

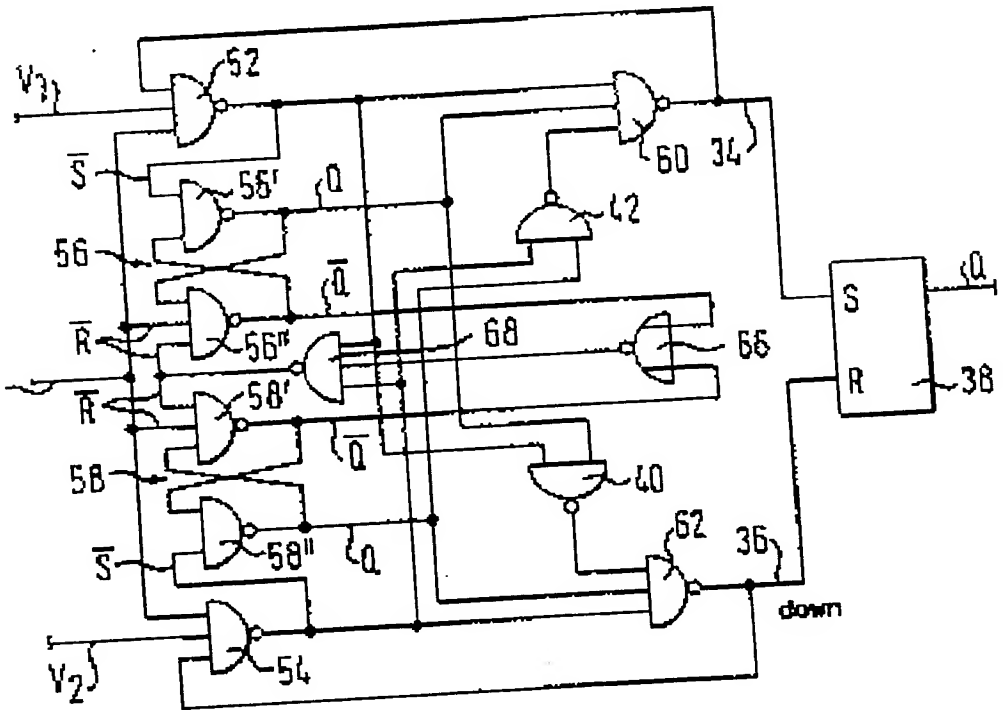
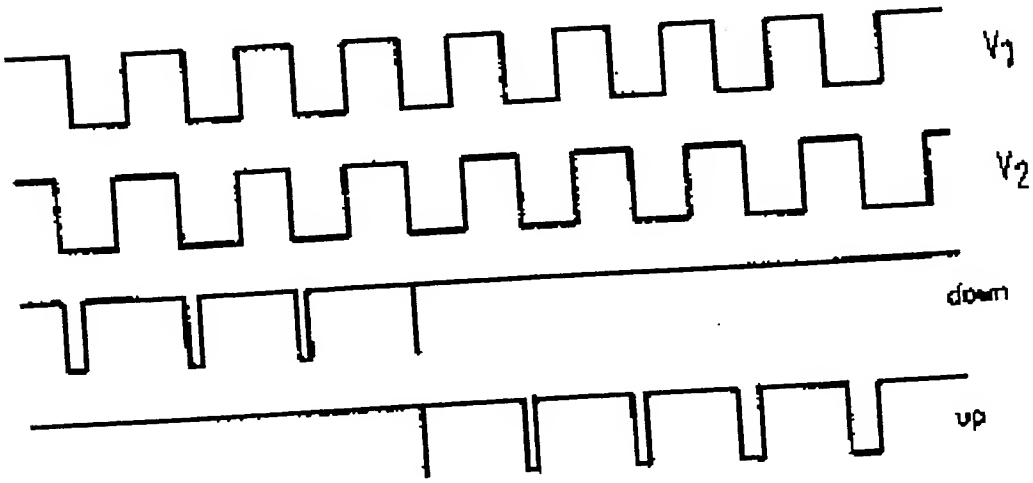

V1
52
S
55'
Q
56
42
Q
R
56''
68
66
S
Q
R
38
58'
58
Q
40
62
58''
Q
36
S
down
V2
54

FIG. 9


V1
V2
down
up

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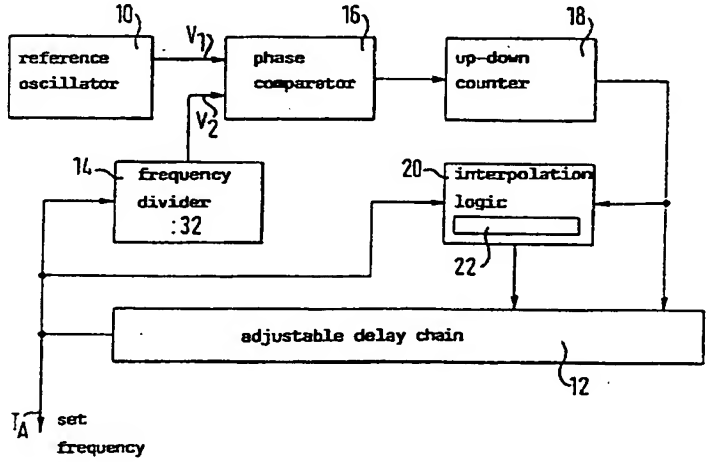
(54) A clock generator and phase comparator for use in such a clock generator

(57) 1. A clock generator contains a reference oscillator (10), a digital closed delay chain (12), a digital frequency divider (14) and a digital phase comparator (16). The frequency divider (14) is connected between the output of the adjustable delay chain (12) and one input of the phase comparator (16). The output of the reference oscillator (10) is connected to a further input of the phase comparator (16). Between the output of the phase comparator (16) and the delay chain (12) a digital up-down counter (18) is connected, the counting direction of which is determined by the output signal of the phase comparator (16) and by means of which the corresponding length of the delay chain (12) is adjustable.

FIG. 1



EP 0 657 796 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 11 9499

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 528 283 A (SONY CORP) 24 February 1993 * column 4, line 4 - column 7, line 51; figures 2,3 * ---	1	G06F1/08 H03L7/099 H03D13/00
A	JP 05 102 801 A (NIPPONDENSO CO LTD) 23 April 1993 * the whole document * ---	1-11	
A,P	& US 5 331 294 A (WATANABE ET AL.) 19 July 1994 * column 2, line 40 - column 5, line 46 * * column 6, line 42 - column 13, line 40; figures * -----	1-11	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03L

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
THE HAGUE	25 June 1997	BALBINOT H.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 94 11 9499

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☒ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

1 - 14

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

EP 94 11 9499 - B -

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions, or groups of inventions, namely:

1. Claims 1-14 : A clock generator.
2. Claims 15-18 : A digital phase comparator.